Title: Vacuum packaged micromirror arrays and methods of manufacturing the same

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Technical Field

[0001]   This invention relates to packaged micromirror arrays and methods of manufacturing the same. Such arrays have applications in spatial light modulators.

Background Art

[0002]   Electromechanical micromirror devices have drawn considerable interest because of their application as spatial light modulators (SLMs). A spatial light modulator requires an array of a relatively large number of such micromirror devices. In general, the number of devices required ranges from 60,000 to several million for each SLM. Despite significant advances that have been made in recent years, there is still a need for improvement in the performance and manufacturing yields of electromechanical micromirror devices.

[0003]   An example of an early generation prior art device is disclosed in US 4592628. US 4592628 describes an array of light reflecting devices on a substrate. Each device comprises a hollow post and a deflectable polygonal mirror attached thereto. Each mirror acts as a deflectable cantilever beam. The mirrors are deflected by a beam of electrons from a cathode ray tube. Fig. 4 of

US 4592628 shows the micromirror device enclosed in the evacuated interior of a cathode ray tube.

[0004]   A 1st generation Texas Instruments, Inc. (TI) device is described in US 4662746. A micromirror is suspended by 1 or 2 hinges. If suspended by 1 hinge, the micromirror deflects like a cantilever beam. If suspended by 2 hinges, the micromirror deflects like a torsion beam. Addressing electrodes are located below the micromirrors and addressing circuits are located at the same level in the substrate as the addressing electrodes.

[0005]   A 2nd generation TI device is described in US 5583688. A 2nd generation TI device is one in which the torsion hinge is at a different level than the reflective mirror. As described more fully in US 5583688, the mirror is supported by a mirror support post, which is attached to the torsion hinge by a yoke. In US 5583688, the mirrors are actuated by electrostatic forces between the mirror and address electrodes. The device is designed such that the mirror edge do not touch the address electrodes. Instead, the yoke edge touches the yoke landing site. The fill factor is relatively high because the CMOS circuits and torsion hinges are hidden under the mirror. Metallic pads are placed along at least one peripheral edge of the array for making electrical connections. In the conventional art, the electrical connections are made by wire bonding.

[0006]   Micromirrors that are described in US 4662746 and US 5583688 are fabricated on top of CMOS circuits. There may be manufacturing problems associated with the fabrication of micromirrors on top of CMOS circuits. This issue is discussed in US 5216537. In this patent, it is discussed that the surface

of the CMOS chip has certain manufacturing artifacts, namely aluminum hillocks, pinholes, nonplanar surfaces, and steep sidewalls in the protective oxide at edges of aluminum leads. In response to these problems, US 5216537 discloses an improved architecture in which an air gap is provided between the top surface of the CMOS chip and the mirror addressing electrodes. A further advantage of this approach is that because of the low dielectric constant of air, parasitic coupling between the CMOS and the micromirror is reduced.

[0007]   The placement of CMOS circuits directly under the micromirrors is also responsible for problems of photosensitivity. As discussed in US 6344672, it was found that the CMOS memory cells are unstable in a high-intensity light environment. The patent provided an active collector region in which photogenerated carriers could recombine before reaching the addressing electrode.

[0008]   Reflectivity, Inc. (Sunnyvale, California) is also known to be developing micromirror devices. As disclosed in US 5835256, the aforementioned problems associated with placing CMOS and micromirrors on the same substrate are solved by placing the micromirrors and CMOS on different substrates. In other words, a hinge and a micromirror are fabricated on an optically transparent substrate, such that the optically reflective surface of the micromirror is proximate the optically transparent substrate. Addressing circuits including mirror addressing electrodes are fabricated on a 2nd substrate (typically silicon) and the 2 substrates are bonded together with a predetermined gap between the micromirror and the addressing electrodes.

[0009] However, a difficulty with the architecture of US 5835256 is that the gap between the mirror and mirror addressing electrodes is difficult to control. Since the actuation force is superlinearly dependent on this gap, it is imperative to achieve uniform gap over the entire array to obtain uniform performance characteristics. As discussed in US 2003/0134449 A1, 2nd and higher order adjustments in the gap may be needed in the manufacturing process. Such adjustments make the manufacturing process more complicated. It would be preferable to have a device architecture in which the mirror address electrodes and mirrors are disposed on the same substrate.

[0010] US 6538800 discusses the use of amorphous silicon as a sacrificial layer in fabricating a micromirror device. It is shown that amorphous silicon can be deposited for this purpose by LPCVD in a quartz tube of a Tylan furnace. It is also shown that a xenon difluoride etch process can be used to etch amorphous silicon with a selectivity of 100 to 1. Therefore, amorphous silicon can be used successfully as a sacrificial layer in addition to photoresists, silicon oxide, silicon nitride, and silicon oxynitride.

[0011] In many cases, there is a need to encapsulate MEMS devices in a vacuum. There is the example of aforementioned US 4592628 in which the micromirror device is encapsulated in the vacuum of a cathode ray tube. US 6479320 describes the vacuum packaging of MEMS devices such as infrared bolometers, gyros, and accelerometers. Instead of packaging individual chips, the entire wafer is packaged simultaneously. This is accomplished by the following steps:

1) Fabricate MEMS devices on a device wafer

2) Form sealing rings at the periphery of each die on the device wafer, where the sealing ring comprises a layer of silicon nitride (for electrically isolating the underlying electrical leads) followed by a solder comprising a 1st layer of titanium, a 2nd layer of palladium, and a 3rd layer of gold.

3) Similarly form sealing rings on the lid wafer.

4) The lid wafer and device wafer are aligned to each other and evacuated.

5) The wafers are heat treated to form a seal.

Note that US 6479320 describes the vacuum sealing of a device wafer to a lid wafer, where the MEMS devices are disposed on the device wafer.

[0012] A preferred sealing method is glass frit sealing because it forms a leak-free seal over non-planar surfaces. Glass frit compositions are well known in the art. Generally a glass frit composition comprises a glass powder, a solvent, a binder, and optionally other additives. Suitable glass powders include PbO, B_2O_3, silica (SiO_2), alumina (Al_2O_3), and others. Acrylics may be used as binders. In a conventional method of sealing 2 substrates, glass frit compositions are coated at the desired bond line on one or both substrates. Methods for coating the glass frit composition include deposition from a nozzle dispenser, screen printing, tape casting, molding, and extrusion. The formulation of the glass frit composition is at least partially dependent upon the desired width and thickness of the bond line.

[0013] US 6583079 describes glass frit compositions that can be sealed at relatively low temperatures of 410 to 430 °C with relatively short curing times of 5 to 20 minutes. Glass powders according to US 6583079 have glass transition

temperatures ranging from 296 to 321 °C, and softening temperatures ranging

from 338 to 398 °C. The glass powders essentially consist of 75 - 90 % PbO, 7 -

20 % B_2O_3, 0 - 8 % ZnO, 0 - 5 % SiO_2, and 0.1 - 8 % Al_2O_3 + Fe_2O_3.

[0014]   US 6537892 discloses a glass frit sealing process for MEMS devices

such as accelerometers, sensors, and actuators. The process relates to the

formation of a seal between a device wafer containing MEMS devices and a lid

wafer. Preferred methods of curing the glass frit composition are described.

There are 2 important features to this invention. Firstly, the glass frit composition

contains a particular filler material that establishes a stand-off distance between

the 2 wafers, where the filler material has a higher melting point than the glass frit.

Secondly, the wafers are provided with recessed areas adjacent bond areas for

accommodating excess glass frit material. The 2nd innovation is useful for

limiting the width of the bonding line. Limiting the width of the bonding line is

important when the bonding line is being formed on a high cost, device quality

wafer.

[0015]   Typically, an exhaust tube is placed at the periphery of the substrate so

that it crosses the bonding line. Initially, there is a 1st heat treatment to remove

the solvent and binder. The temperature of the 1st heat treatment may be in the

range of about 100 C to 300 °C, i.e. temperatures that are sufficient to vaporize

the binder and solvent but do not melt the glass powder. The substrates are

aligned and are heated to melt the glass frit to form a seal around the bonding

line and the exhaust pipe. The assembly is evacuated through the exhaust pipe,

and when the evacuation is complete, the exhaust pipe is sealed. In an

alternative method, an evacuation pipe is sealed to the outer surface of the rear

substrate using frit glass. Such a method is described, for example, in US

6407501, which describes a sealing method for a plasma display panel (PDP).

[0016]   Sealing methods that do not use exhaust pipes have also been

disclosed. The elimination of the exhaust pipe reduces manufacturing steps and

makes more efficient use of the available space for the electronic device. US

6129603 discloses a sealing method for a field emission display using a low

temperature glass frit. A glass frit with a glass transition temperature of 200 to

250 °C is formed by mixing 2 % to 4 % Q-Pac organic compound with NEG

(Nippon Electric Glass) low temperature glass. The glass frit composition is

deposited along the bonding line on one substrate and the 2 substrates are

assembled. The assembly is evacuated in a vacuum oven and then heated to <

300 °C to melt the glass frit and form a seal.

[0017]   Another sealing method for field emission displays without using

exhaust pipes is disclosed by US 5997378. The preferred glass frit is LS-1014

from Nippon Electric Glass. In this method, a glass frit composition is deposited

along the bonding line. In addition, compressible protrusions of glass frit are also

deposited along the bonding line. In a preferred embodiment, the compressible

protrusions are about 250 microns tall and are located at 25 mm intervals. The

space between the compressible protrusions act as high conductance exhaust

channels during the evacuation step. After the evacuation step, the glass frit is

melted in a high temperature step and the seal is formed. The evacuated

chamber also includes 2 strip of getter material (ST-707 getter strip from SAES),

located along the edge of the display. Metallic particles deposited on the metal foil become reactive when heated. The getter functions to decrease the pressure within the sealed space throughout the lifetime of the display. It was found that the getter was activated above 375 °C.

[0018]   It is known that micromirrors are sensitive to dust, particles, gases, moisture, and other environmental factors. Conventionally, electrical connections to micromirror arrays are made by wire bonding. In prior art devices where the micromirror and addressing circuitry are on the same substrate (e.g. US 4662746 and US 5583688), it would be desirable to form a protective layer on the micromirror array while wire bonds are formed at the periphery of the die. However, since it is not possible to remove the protective layer after the wire bonding, wire bonding must be carried out with neighboring micromirrors unprotected.

[0019]   In micromirror devices where the CMOS and micromirrors are on separate substrates (e.g. US 5835256), the micromirrors may be protected by sealing the 2 substrates before performing the wire bond. However, as discussed above, there are other manufacturing problems that arise from placing the CMOS circuitry and micromirrors on separate substrates.

[0020]   US 6507082 provides a flip-chip assembly method for devices in which the CMOS circuitry and micromirrors are on the same side of the same substrate. Furthermore, the micromirrors are protected in a protective layer during the flip-chip assembly. In summary, the method outlined in US 6507082 is as follows:

1) Form micromirror arrays and addressing circuits on a substrate;

2) Form a protective layer on the substrate and pattern it such that the micromirror arrays are protected and metallic pads are exposed;

3) Deposit solder balls on the metallic pads;

4) Singulate the chips;

5) Flip-chip assemble a chip into the opening of a ceramic substrate;

6) Underfill the gaps between the solder joints with a polymeric encapsulant;

7) Remove the protective layer from the micromirror array; and

8) Attach a lid to the substrate for sealing the package.

This method is an improvement in that flip-chip assembly is used and the micromirror array is protected during assembly. However, a limitation is that although the package is sealed, it is not under vacuum. It should be noted that the interface region between the chip and the package contains both the polymeric encapsulant and the solder ball array. This interface is not intended to maintain a vacuum, and it is not the intention of the patent to provide a vacuum interior.

Summary of the Invention

[0021]   The present invention provides vacuum packaged micromirror arrays and methods of manufacturing them that overcome some of the limitations of the prior art. According to the present invention, a vacuum packaged electromechanical micromirror array comprises a 1st packaging substrate, a 2nd packaging substrate, a device substrate with a 1st surface and a 2nd surface, control circuitry disposed on said 1st surface, and a plurality of micromirrors disposed on said 2nd surface. The vacuum packaged arrays may be 1-

dimensional (linear) or 2-dimensional and may be used as a spatial light

modulators (SLMs). The device substrate resides on the 1st packaging substrate

with electrical connections between them. The micromirror array is sealed in a

vacuum packaged formed by the packaging substrates. According to the present

invention, methods of fabricating vacuum packaged micromirror arrays generally

involve providing a device substrate with a 1st surface and a 2nd surface,

fabricating control circuitry on the 1st surface, fabricating micromirrors on the 2nd

surface, providing a 1st packaging substrate, mounting the device substrate on

the 1st packaging substrate by flip-chip assembly, providing a 2nd packaging

substrate, and sealing the packaging substrate by glass frit sealing. In a

preferred embodiment, control circuits are fabricated using CMOS technology. In

another preferred embodiment, the control circuits on the 1st surface are

protected by a protective layer during the fabrication of micromirrors on the 2nd

surface. In yet another preferred embodiment, the device substrate is a silicon-

on-insulator (SOI) substrate. In yet another preferred embodiment, the 1st

packaging substrate is an insulating substrate such as ceramic or glass, and the

2nd packaging substrate is transparent to electromagnetic radiation.

[0022]   A 1st advantage of the present invention is that it provides improved

dielectric isolation between the control circuit and the micromirror. A 2nd

advantage of the present invention is that provides improved optical isolation of

the control circuit area. This is particularly advantageous when the micromirror

array is used as a spatial light modulator (SLM) and the 1st surface (the

micromirror side) is exposed to high intensity radiation. A 3rd advantage of the

present invention is that it provides improved manufacturing yields because the

control circuit manufacturing processes and micromirror manufacturing

processes can be substantially isolated from each other. In other words,

manufacturing artifacts arising from the control circuit process will not damage

the micromirror because the micromirror is not built on top of the control circuit.

A 4th advantage of the present invention is that the micromirror array is provided

in a vacuum package with electrical connections formed by flip-chip assembly.

As a result, there is a concomitant improvement in manufacturing yield and

reliability and performance of the array during its lifetime. These and other

advantages of the present invention will become apparent from the detailed

description and the claims below.

Brief Description of the Figures

[0023]   Fig. 1 is a schematic diagram of a 4-pixel array of micromirror devices,

comprising control circuits, addressing electrodes, and micromirrors.

[0024]   Fig. 2 is a schematic cross sectional view of a micromirror device in

accordance with the present invention.

[0025]   Fig. 3A is a schematic plan view of a micromirror device in accordance

with a 1st embodiment of the present invention.

[0026]   Fig. 3B is a schematic cross sectional view along line a-b of Fig. 3A.

[0027]   Fig. 4A is a schematic plan view of a micromirror device in accordance

with a 2nd embodiment of the present invention.

[0028]   Fig. 4B is a schematic cross sectional view along line c-d of Fig. 4A.

[0029]   Fig. 5A is a schematic plan view of a micromirror device in accordance with a 3rd embodiment of the present invention.

[0030]   Fig. 5B is a schematic cross sectional view along line e-f of Fig. 5A.

[0031]   Figs. 6A through 6D are schematic plan views of a micromirror device according to a 4th embodiment of the present invention, at varying levels of elevation.

[0032]   Figs. 7A through 7D are cross sectional views illustrating the fabrication steps on a 1st device substrate surface, in accordance with a 4th embodiment of the present invention.

[0033]   Figs. 8A through 8M are cross sectional views illustrating the fabrication steps on a 2nd device substrate surface, in accordance with a 4th embodiment of the present invention.

[0034]   Fig. 9 is a schematic plan view illustrating a micromirror array of rectangular micromirrors according to a 5th embodiment of the present invention.

[0035]   Fig. 10 is a schematic plan view illustrating an array of hexagonal micromirrors in accordance with a 6th embodiment of the present invention.

[0036]   Fig. 11A is a schematic plan view of a micromirror device in accordance with a 7th embodiment of the present invention.

[0037]   Fig. 11B is a schematic cross sectional view along line i-j of Fig. 11A.

[0038]   Fig. 11C is a schematic plan view of a micromirror device in accordance with an 8th embodiment of the present invention.

[0039]   Fig. 12A is a schematic plan view of a 1st packaging substrate in accordance with the present invention.

[0040] Fig. 12B is a schematic plan view illustrating a step in a fabrication

process of a vacuum packaged micromirror array in accordance with the present

invention.

[0041] Fig. 12C is a schematic cross sectional view of a vacuum packaged

micromirror in accordance with the present invention.

Detailed Description of the Invention

[0042] The present invention relates to electromechanical micromirror devices

and arrays of such devices. Shown schematically in Fig. 1 is an array 100

comprising vertical data lines (101 and 102) and horizontal addressing lines (103

and 104), with each intersection of these data and addressing lines forming an

electromechanical micromirror device (105, 106, 107, and 108). Each

micromirror device comprises a micromirror (109, 110, 111, and 112), an

addressing electrode (113, 114, 115, and 116), and an NMOS transistor (117,

118, 119, and 120). Micromirror 109 is shown to be in a deflected state while the

other micromirrors are in their undeflected states. A possible scheme for

addressing the micromirrors is as follows: The micromirrors (109, 110, 111, and

112) are electrically connected to ground. The deflection of a micromirror is

determined by the bias voltage between the micromirror and its addressing

electrode. The desired bias voltage is set by the voltages on the vertical data

lines (101 and 102). The NMOS transistors are turned on by sending a low-high-

low pulse on the addressing lines (103 and 104), which results in the bias

voltages being stored between the micromirrors and addressing electrodes.

[0043] While array 100 (Fig. 1) has been shown to consist of 4 micromirror

devices, an array may typically consist of greater than 60,000 micromirror

devices and may be used as a spatial light modulator (SLM). Furthermore, while

Fig. 1 shows a plurality of micromirror devices disposed in a 2-dimensional array,

1-dimensional (linear) array are also possible.

[0044] The circuitry as shown in Fig. 1 comprises the following:

1) micromirrors;

2) micromirror addressing electrodes; and

3) control circuitry.

In the particular case of Fig. 1, control circuitry consists of the vertical data lines

(101 and 102), horizontal addressing lines (103 and 104), NMOS transistors (117,

118, 119, and 120), and electrical connections among them. In general, control

circuitry is understood to mean any circuitry that is provided to control the

application of bias voltages between a micromirror and its addressing electrode.

As shown in Fig. 1, the control circuitry comprised NMOS transistors. However,

it should be understood that the control circuitry could comprise other types of

circuits, including CMOS circuits, PMOS circuits, bipolar transistor circuits,

BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film

transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits,

SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP

transistor circuits, CdSe transistor circuits, organic transistor circuits, and

conjugated polymer transistor circuits.

[0045] Some of the important concepts of the present invention are illustrated

schematically in Fig. 2. A device substrate 201 has a bottom surface on which

control circuitry 202 is fabricated. Micromirror 203 and addressing electrodes

204 and 205 are fabricated on the top surface of substrate 201. For simplicity,

support structures for supporting micromirror 203 are not shown. Electrical

connections between the addressing electrodes (203 and 204) and control

circuitry 202 are provided by electrical routing lines 206 and 207. The electrical

routing lines 206 and 207 may be in the form of vias in the device substrate 201

with metallization in these vias. The device substrate may be selected from

among the following: silicon-on-insulator (SOI), silicon, polycrystalline silicon,

glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP.

In general, the choice of device substrate should be consistent with the choice of

control circuit technology. For example, a silicon-on-insulator substrate may be

suitable for CMOS circuits, and a glass substrate may be suitable for amorphous

silicon thin film transistor circuits.

[0046]   As discussed with reference to Fig. 1, a micromirror device comprises a

control circuitry, a micromirror, and addressing electrodes. Fig. 3A is a

schematic plan view of a portion of a micromirror device 300 in accordance with

a 1st embodiment of the present invention. Micromirror 301 is shown with its

reflective side facing towards the reader. The reflective side of micromirror 301

is substantially planar, with neither recessions nor protrusions. Micromirror 301

is supported by a torsion hinge 302. In the case that micromirror portion 300 is

disposed in an array for a spatial light modulator (SLM), arrow 303 indicates the

projection of the incident light propagation direction on the device substrate plane.

Note that micromirror 301 has 4 edges and no edge is perpendicular to arrow

303. Fig. 3B is a schematic cross sectional view along line a-b through torsion hinge 302. Micromirror 301 and torsion hinge 302 are supported by support structures 304 and 305, which are disposed on device substrate 306. Since the micromirror deflects by torsion, the axis of rotation of the micromirror is approximately perpendicular to arrow 303.

[0047] Fig. 4A is a schematic plan view of a portion of a micromirror device 400 in accordance with a 2nd embodiment of the present invention. Micromirror 401 is shown with its reflective side facing towards the reader. The reflective side of micromirror 401 is substantially planar, with neither recessions nor protrusions. Micromirror 401 is supported by a beam 402. In the case that micromirror device 400 is disposed in an array for a spatial light modulator (SLM), arrow 403 indicates the projection of the incident light propagation direction on the device substrate plane. Note that micromirror 401 has 4 edges and no edge is perpendicular to arrow 403. Fig. 4B is a schematic cross sectional view along line c-d through beam 402. Beam 402 is supported by support structure 404, which is disposed on device substrate 406. In contrast to micromirror 301 (Figs. 3A and 3B), the axis of rotation of micromirror 401 is approximately parallel to arrow 403.

[0048] Fig. 5A is a schematic plan view of a portion of a micromirror device 500 in accordance with a 3rd embodiment of the present invention. Micromirror 501 is shown with its reflective side facing towards the reader. The reflective side of micromirror 501 is substantially planar, with neither recessions nor protrusions. In the case that micromirror device 500 is disposed in an array for a spatial light

modulator (SLM), arrow 503 indicates the projection of the incident light

propagation direction on the device substrate plane. Fig. 5B is a schematic cross

sectional view along line e-f. Micromirror 501 is supported by a support structure

504, which is disposed on device substrate 506. The axis of rotation of

micromirror 501 is approximately parallel to arrow 503.

[0049] An important difference between between micromirror device 400 (Figs.

4A and 4B) and micromirror device 500 (Figs. 5A and 5B) is that in device 400,

there is a beam 402 which supports the micromirror 401 on the support structure

404, whereas in device 500, the micromirror is positioned directly on support

structure 504. Therefore, in Fig. 5A, the top side 502 of support structure 504 is

visible in the plan view.

[0050] Figs. 6A through 6D are schematic plan views of a micromirror device

600 accoding to a 4th embodiment of the present invention, at varying levels of

elevation. Fig. 6A shows the reflective side (top side) of a micromirror 601. In

the case that micromirror device 600 is disposed in an array for a spatial light

modulator (SLM), arrow 602 indicates the projection of the incident light

propagation vector on the device substrate plane. Arrow 602 is not

perpendicular to any of the 4 sides of micromirror 601. Arrow 602 is shown to be

approximately 45 degrees from the leading edges of micromirror 601. The

reflective side of micromirror 601 is is substantially flat, with neither recesses nor

protrusions. As a result, there are no diffraction effects that would be caused by

recesses or protrusions in the micromirror.

[0051]   Fig. 6B shows a plan view that is analogous to Fig. 6A except that micromirror 601 has been removed. Addressing electrodes 603 and 604, micromirror support structure 605, and torsion hinge 606 are visible. Torsion hinge 606 supports micromirror support structure 605. Addressing electrodes 603 and 604 are electrically connected to control circuitry which is not shown. Micromirror 601 is actuated by electrostatic forces between it and one or both of the addressing electrodes 603 and 604. Fig. 6C shows the result of removing the mirror support structure 605.

[0052]   Fig. 6D shows the result of removing torsion hinge 606. Torsion hinge support structures 607 and 608 are shown. Figs. 7A through 7D and 8A through 8M show a fabrication sequence of a micromirror device using a cross sectional view along the line g-h. In many cases, the micromirror device would be fabricated in an array for use as a spatial light modulator. Therefore, although Figs. 7A through 7D and 8A through 8M illustrate the fabrication of a single micromirror device, it should be understood that the teachings can be extended to the fabrication of an array of micromirror devices.

[0053]   Figs. 7A through 7D illustrate a fabrication sequence on the control circuitry side. Fig. 7A shows a silicon-on-insulator (SOI) substrate 700 comprising an epitaxial top silicon layer 703 with a thickness typically ranging from 50 nm to 600 nm, an intermediate insulator layer 702 with a thickness typically ranging from 50 nm to 2 μm, and a bottom silicon layer 701 with a thickness of around 775 μm. One of the advantages of SOI over silicon substrates is the improved dielectric isolation. In the case of the present

invention, the SOI substrate is used to improve the dielectric isolation of the control circuitry and micromirror portion.

[0054]   Fig. 7B shows the formation of control circuitry 704 on epitaxial layer 703 of the SOI substrate 700. In general, any integrated circuit technology can be considered for fabricating the control circuitry. For example, CMOS circuitry may be used. However, for applications requiring high frequency or high voltages, BiCMOS or DMOS circuitry may be used.

[0055]   Fig. 7C shows the step of forming a trench 705 through the top epitaxial silicon layer 703 and insulator layer 702, using standard patterning and an anisotropic etch. The anisotropic etch is stopped before the trench 705 reaches the bottom silicon layer 701. This is followed by a metal deposition and patterning step (Fig. 7D) which forms an electrical connection 706 between the control circuitry and the trench. It should be understood that this metal could be any metal that is used in semiconductor fabrication, such as Al alloy, and methods of metal deposition include sputtering, thermal evaporation, and CVD.

[0056]   At this point the process steps on the control circuitry side are complete. It may be preferable to form a protective layer on the control circuitry side. Figs. 8A through 8M illustrate a fabrication sequence on the micromirror side. The control circuitry side is mounted on a carrier to securely hold the substrate for the subsequent step (Fig. 8A) of backgrinding and chemical mechanical polishing (CMP) of the back silicon layer 701 to expose the intermediate insulator layer 702.

[0057]   As shown in Fig. 8B, insulator layer 702 is pattered to form a trench 801,

thereby completing the via that had been started in the step of Fig. 7C. Another

metallization (deposition and patterning) step (Fig. 8C) forms addressing

electrodes 802 that are electrically connected, through via 801, to control

circuitry 704.

[0058]   After the formation of the addressing electrodes 802, the torsion hinge

and its support structures are formed. An embodiment of this process is

illustrated in Figs. 8D through 8H. An amorphous silicon sacrificial layer 803 is

deposited by LPCVD (Fig. 8D). Other suitable methods of depositing amorphous

silicon are PECVD, catalytic CVD (also known as hot wire CVD), and sputtering.

As discussed in the Background Art section, xenon difluoride can be used to etch

amorphous silicon with a selectivity of 100 to 1. Other possible sacrificial layers

are photoresists, silicon oxide, silicon nitride, and silicon oxynitride. As shown in

Fig. 8E, a photolithographic patterning and anisotropic etching step is carried out

to form a recess 804 where the torsion hinge will be formed. Then, another

photolithographic patterning and anisotropic etching step (Fig. 8F) is carried out

to form holes 805 and 806 where the torsion hinge support structures will be

formed. The holes 805 and 806 for the torsion hinge support structures reach

the intermediate insulator layer.

[0059]   As shown in Fig. 8G, a layer 807 of structural material is deposited. For

example, the structural material may be an Al alloy comprising 0.2 % Ti, 1 % Si,

and the remainder Al. A preferred method of depositing this Al alloy is sputter

deposition. A metal is chosen for the structural material because the micromirror

is typically held at ground potential. As shown in Fig. 8H, structural material layer 807 is patterned to form a torsion hinge 808 and torsion hinge support structures 809 and 810. Torsion hinge 808 and torsion hinge support structures 809 and 810 are at least partially embedded in sacrificial layer 803.

[0060] A micromirror support structure is placed between the torsion beam and the micromirror. As shown in Fig. 8I, a metal layer is deposited and then patterned to provide a micromirror support structure 811 on torsion beam 808. The metal may be an Al alloy comprising 0.2 % Ti, 1 % Si, and the remainder Al. A preferred method of depositing this Al alloy is sputter deposition. Another layer of sacrificial amorphous silicon is deposited (Fig. 8J) such that the micromirror support structure 811 is fully covered by sacrificial layer 803. A chemical mechanical polishing (CMP) process is carried out to planarize the surface such that the following requirements are satisfied:

1) the top of the micromirror support structure 811 is exposed and planar;

2) the sacrificial layer 803 is planar; and

3) the top of the micromirror support structure 811 and the top of the sacrificial layer 803 are at the same level.

In this description, top is understood to mean bottom on the drawing page. The result of the planarization step is shown schematically in Fig. 8K.

[0061] A metallic layer is deposited and patterned to form a micromirror 812 as shown in Fig. 8L. The metal may be an Al alloy comprising 0.2 % Ti, 1 % Si, and the remainder Al. A preferred method of depositing this Al alloy is sputter deposition. The micromirror 812 is connected to the micromirror support

structure 811. A xenon difluoride etch is carried out to remove the amorphous silicon sacrificial layer (Fig. 8M).

[0062] In the foregoing discussion the preferred micromirror comprised a metallic coating. However, it is also possible to construct a micromirror out of multiple alternating layers of higher refractive index and lower refractive index dielectrics. This may be accomplished by using silicon oxide and silicon nitride. Therefore, if an Al mirror has a reflectivity of 92 %, the reflectivity can be increased to over 95 % by first depositing 68 nm of silicon nitride (n = 2.0) and then depositing 96 nm of silicon dioxide (n = 1.46).

[0063] In the foregoing discussion of Figs. 8G to 8M, all of the structural members (torsion hinge, torsion hinge support structures, micromirror, micromirror support structures) were metallic. Alternatively, it is possible to use a dielectric (e.g. hardened photoresist, silicon oxide, silicon nitride, silicon oxynitride) that has been covered with a metallic sheath as a structural member, as described more fully in US 5631782.

[0064] Typically, micromirror devices are incorporated into an array. Fig. 9 shows a 2-dimensional array 900 of rectangular micromirrors (901, 902, 903, and 904), according to a 5th embodiment of the present invention. Arrow 906 indicates the projection of the incident light propagation vector on the mirror plane (device substrate plane). The reflective side of the micromirror has no edges that are perpendicular to arrow 906. This is a configuration that reduces diffraction into the acceptance cone of the optical system. Another possible shape for a micromirror is a hexagon, shown being disposed in an array 1000 in

Fig. 10, according to a 6th embodiment of the present invention. There are

micromirrors 1001, 1002, 1003, 1004, and 1005. Arrow 1006 indicates the

projection of the incident light propagation vector on the mirror plane (device

substrate plane). The reflective side of the micromirrors has no edges that are

perpendicular to arrow 1006.

[0065]   A 7th embodiment of the present invention is explained with reference

to Figs. 11A and 11B. Fig. 11A is a schematic plane view of a micromirror device

1100, comprising a micromirror 1101 and a micromirror support structure 1104.

Arrow 1103 indicates the projection of the incident light propagation vector on the

micromirror plane (device substrate plane). The reflective side of the micromirror

has no edges that are perpendicular to arrow 1103. The reflective side of

micromirror 1101 is substantially planar, with neither recessions nor protrusions.

Fig. 11B is a schematic cross sectional view along line i-j of Fig. 11A. An

addressing electrode 1108 is located under micromirror 1101 and on top of

device substrate 1106. Furthermore, a stopper 1107 has been provided. The

purpose of stopper 1107 is to prevent micromirror 1101 from contacting

addressing electrode 1108 under deflection. This may cause an electrical short.

Instead, micromirror 1101 contacts stopper 1107. In cases where a micromirror

deflects in 2 directions from its undeflected state, it is possible to provide 2

stoppers with 1 stopper for each direction of deflection.

[0066]   Fig. 11C illustrates a modification to micromirror device 1100 in

accordance with an 8th embodiment of the present invention. Fig. 11C is a plan

view of a micromirror device 1100 comprising a micromirror 1101, a support

structure 1104, and a stopper 1107. In its undeflected state, the reflective side of micromirror 1101 has no edges that are perpendicular to arrow 1103. When the micromirror 1101 is actuated, the region 1108 of micromirror 1101 that is adjacent to support structure 1104 gets deflected. Therefore, an edge that is perpendicular to arrow 1103 may appear in region 1108. In order to reduce diffraction effects from this edge, it is possible to coat region 1108 with a light absorbing material. A preferred light absorbing material is a black dye.

[0067]   In a preferred embodiment, a micromirror array is packaged in a vacuum package and electrical connections are formed by flip chip assembly. An insulating substrate such as glass or ceramic is provided as shown in Fig. 12A. Fig. 12A is a schematic plan view of a 1st packaging substrate 1200. Substrate 1200 has a plurality of metallic terminals 1202 and a plurality of lead wires 1201, such that the terminals 1202 are configured to mate with the metallic terminals of the control circuitry of the micromirror array. The device wafer that contains the micromirror array is singulated. A micromirror array chip is aligned with the 1st packaging substrate and mounted by flip chip assembly.

[0068]   Fig. 12B shows a schematic plan view of the 1st packaging substrate 1200 after the micromirror array chip has been mounted and a glass frit composition has been coated around the array. Micromirror array chip 1202 is mounted with the control circuitry side facing the 1st packaging substrate and the micromirror side facing the reader. A glass frit composition is coated at the bonding line 1203 that surrounds the micromirror chip array 1202. Portions of lead wires 1201 are located outside the bonding line 1203. An evacuation tube

1204 is provided and a glass frit bonding line is formed around it (1205 and 1206).

[0069]   Portions of lead wires 1201 are located outside the bonding line 1203.

It is preferable to use Dumet to form the lead wires 1201 in order to form a leak-

tight reliable seal. Dumet is an alloy that is substantially approximately 42 %

nickel and 58 % iron, but with the allowance that there may often be about 1 % or

less of a combination of various elements such as silicon, carbon, and

magnesium. Dumet has a relatively high coefficient of thermal expansion (about

$90 \times 10^{-7}/$ °C). The surface of the Dumet wire may be deliberately oxidized to

improve the adhesion to the glass frit.

[0070]   Fig. 12C is a schematic cross sectional view of an assembled package

1208 along line k-l of Fig. 12B. A 2nd packaging substrate 1207 (lid substrate) is

provided to assemble the package. In Fig. 12B, the micromirrors are facing

toward the reader (out of the page). Therefore, the 2nd packaging substrate

1207 (lid substrate) should be transparent to electromagnetic radiation, and could

preferably be glass, quartz, or sapphire. If the micromirror array is to be used to

modulate infrared light, it may be acceptable to use silicon as the 2nd packaging

substrate.

[0071]   It is generally preferable to establish a stand-off distance between the 2

packaging substrates. This may be accomplished by providing a frame (for

example made out of ceramic) and placing the frame at bonding line 1203. The

thickness of the frame approximately determines the stand-off distance.

Preferably the glass frit composition is coated on both sides of the frame.

Alternatively, the stand-off distance may be fixed by coating the glass frit

composition, heating the composition to remove the solvent and binder, and planarizing the glass frit coating. Alternatively, the stand-off distance may be established by using a glass frit composition comprising a glass frit and a particular filler material with a melting point higher than that of the glass frit, as described in the Background Art section.

[0072] The packaging substrates are assembled and the assembly is heat treated at a temperature that melts the glass frit. The assembly is evacuated and then the evacuation tube is sealed.

[0073] The method illustrated in Fig. 12B shows an evacuation tube between the packaging substrates. However, it is also possible to seal the evacuation tube on the 1st packaging substrate. As discussed in the Background Art section, it is also possible to form the vacuum assembly without using an evacuation tube. For example, the assembly may be evacuated before the heat treatment that melts the glass frit seals the bonding line.

[0074] It is preferable to obtain a vacuum package where the pressure is less than about 1×10^{-4} torr, and it is more preferable to achieve less than about 1×10^{-6} torr. It is known to provide a getter material in the interior of a vacuum package to maintain good vacuum during the lifetime of the array. With reference to Fig. 12B, the getter material should be positioned somewhere within the interior of bonding line 1203. However, it may not be preferable to place it in the region between micromirror array 1202 and 2nd packaging substrate (lid substrate) because of primarily 2 reasons: 1) it may block light to or from micromirror array 1202; and 2) when the getter is activated at high temperature,

the getter material may sublime and form deposits on the micromirrors or other

parts of the array.

[0075]   In a preferred embodiment, the interior of the region bounded by the

bonding line 1203 should be divided into 2 regions: 1) a 1st region occupied by

micromirror array chip 1202; and 2) a 2nd region occupied by a getter material.

Normally, the 1st region should be substantially bigger than the 2nd region. The

2 regions should be separated by a non-sealing barrier, such that gas diffusion

between the regions is allowed.